REMARKS

Claims 1-8, 14, 16-19, 31, and 32 are pending. Claims 1-8, 14, 16-19, 31, and 32 are rejected. Claims 1, 14, 17, 31, and 32 are amended. No new matter is added.

Examiner Interview Summary

Applicants respectfully thank the Examiner for the courtesies extended during a telephonic interview conducted with Nishitkumar V. Patel on July 9, 2010. During the interview, claims 1 and 14 were discussed in light of Killian et al. (U.S. Patent No. 5,420,992) ("Killian"). Applicants explained to the Examiner that Killian does not disclose "the single piece of common subcircuitry configured to perform sign extensions of an immediate field in the non-branch instructions and to be reused to perform sign extensions of an immediate field having units of bytes in the branch instructions to calculate a target address for the branch instructions" as called for by claim 1. Rather, Killian discloses in Figure 3C, two different blocks of sign extension circuits. The Examiner indicated that he would be willing to consider the above-made amendments to claims 1 and 14. No agreement was reached.

Section 102 Rejection

Claims 1-8 are rejected under 35 U.S.C. § 102(b) as being anticipated by Killian et al. (U.S. Patent No. 5,420,992) ("Killian"). Applicant respectfully traverses this rejection.

Killian discloses an address unit and address translation circuit, shown below in Figure 3C.